REMARKS

Claims 1, 13-15, and 17-21 are pending in the present application, and claims 2-12 and 16 having been cancelled herein. The Office Action and cited references have been considered. Favorable reconsideration is respectfully requested.

Claims 1, 2, 4, 6-9 were rejected under 35 U.S.C. § 102(a) as being anticipated by Hartlieb (U.S. Patent Publication No. 20040019802). This rejection is respectfully traversed for the following reasons.

Claim 1 recites method for securing a computer system which comprises at least a code interpretation module and memory capacities for storing an interpreted code having measurable physical imprints wherein in order to make more difficult attacks based on physical measurements or requiring synchronization with said interpreted code, the method comprises the steps of providing at least two different implementations for at least one instruction of the interpreted code, the different implementations each requiring a different execution time and/or having a different physical imprint while providing an identical result; selecting one of the different implementations to be executed before each execution of the instruction; and executing the determined different implementation. This is not taught, disclosed or made obvious by the prior art of record.

According to the claimed invention, several executions to the determined instruction within the same interpreted code may be performed by several different implementations.

In contrast, Hartlieb discloses a method for increasing the security of a CPU based on the insertion of selected dummy code sequences into the original code. The code sequences

can be selected randomly and inserted in randomly selected positions in the original code. This feature is clearly explained in paragraph 0017. In paragraph 0019, Hartlieb states that no change of the state of the CPU is caused by the code sequence inserted on a random basis, nor by the plurality of code sequences selected and inserted on a random basis, which solely act as placeholders or dummy code sequences. This paragraph does not suggest a step of providing at least two different implementations for at least one instruction of the interpreted code and a step of implementing the instruction which consists of selecting one of the different implementations to be executed at run time.

At least for these reasons, rejection of newly amended claim 1 under 35 U.S.C. § 102(a) as being anticipated by Hartlieb is believed to be overcome.

Claims 5 and 10 were rejected under 35 U.S.C. §103 as being unpatentable over Hartlieb in view of Collberg (U. S. Patent No. 6,668,325). Cancellation of claims 5 and 10 have rendered this rejection moot.

In view of the above amendment and remarks, Applicant respectfully requests entry of the proposed amendment and reconsideration and withdrawal of the outstanding rejections of record. Applicant submits that the application is in condition for allowance and early notice to the effect is most earnestly solicited.

If the Examiner has any questions, he is invited to contact the undersigned at 202-628-5197.

Respectfully submitted,

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